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EXAMINER	
JEFFERSON, QUOVAUNDA	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/747,621	LEE, BYEONG RYEOL	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 13, 2007 has been entered.

Claim Objections

Claim 4 is objected to because of the following informalities. Appropriate correction is required.

Claim 4 recites the limitation of "...forming the second type well with shallow junction... and an entire region of the device isolation structure between the first type well with shallow junction" in lines 12-14. Examiner is unsure as to what this is referring to since claim fails to state what this second type well with shallow junction is between. Is it between two first type wells with shallow junctions or between two device isolation layers? Examiner would like a clarification as to the meaning of this claim, which

includes where this limitation is located in the specification and which figure the claim is referring. For examination purposes, Examiner will explain between the areas this second type well with shallow junction is located.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smayling et al, US Patent 5,348,895, in view of Yoo et al, US Patent 5,858,830 and Bohr et al, US Patent 5,091,332 (as cited in previous office actions).

Regarding claim 1, Smayling teaches a method of forming device isolation structures in an embedded semiconductor device comprising the steps of providing a semiconductor substrate **150** having a first area **147** for a power device and a second area **139, 140** for a logic device, forming a first device isolation region **210** in the first area, forming a first type well **171** with deep junction by diffusion of ions in the first area forming a device isolation region **210** in a second area of the semiconductor substrate, forming a first type well **171** with shallow junction in peripheral regions of the device

isolation structure (**210 on left side of area 139)** and a region between the device isolation structure (**210 on right side of area 147)** and the device isolation structure (**210 on left side of area 139)**, forming a second type well **161, 190** with shallow junction in peripheral regions of the device isolation structure (**210 in area 147)** and a region of the device isolation structure (**210 in area 140)**, and defining first and second type active regions (**areas between isolation regions 210**) on the semiconductor substrate (see figure 2i, table 1, and column 11, lines 10-35).

Smayling fails to teach forming a device isolation region through partial oxidation and forming a second device isolation with a trench in the second area of the semiconductor substrate.

Yoo teaches forming a device isolation region through partial oxidation (abstract and column 1, lines 40-43) by teaching that traditional memory cells have been fabricated using thermally grown field oxide regions by a thermal oxidation, and forming a second device isolation **11** with a trench in the second area **2** of the semiconductor substrate (column 1, lines 40-47 and figure 7) by teaching the formation of a trench isolation formation within a MOSFET logic devices and field oxide regions within a memory devices because while field oxides offers acceptable junction leakage needed for memory type devices, trench isolations regions offers greater protection against latch0up phenomena than the LOCOS and field oxide counterparts.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yoo with that of Smayling because traditional memory cells have been fabricated using thermally grown field oxide regions by a thermal oxidation and while field oxides offers acceptable junction leakage needed for memory type devices, trench isolations regions offers greater protection against latch-up phenomena than the LOCOS and field oxide counterparts.

Smayling and Yoo fail to teach forming the first type well during the same partial oxidation process as the forming the first device isolation region.

Bohr teaches forming the first type well during the same partial oxidation process as the forming the first device isolation region(column 2, lines 7-10 and column 3, line 63 to column 4, lines 18) by teaching the formation of a field oxide region during the oxidation step, which simultaneously causes the implanted ions to diffuse during the formation of the field oxide. Later, another high temperature step is performed to further diffuse the ions into the substrate. The advantage of these steps is that the second high temperature step causes further diffusion of the ions to form a well without further growing the field oxide step.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Bohr with that of Smayling and Yoo because the advantage of using a wet oxidation process/dry temperature process formation is that

that the second high temperature step causes further diffusion of the ions to form a well without further growing the field oxide step.

Regarding claim 3, Smayling teaches the first type well is an n-type well and the second type well is a p-type well (figure 2k).

Regarding claim 4, Smayling teaches a method of forming device isolation structures in embedded semiconductor device comprising of providing a semiconductor substrate **150** having a first area **147** for a power device in which a first type impurity ions **171** are implanted and a second area **139, 140** for a logic device, forming a first device isolation region **210** in the first area **147**, forming a first type well **171** with deep junction by diffusing the ions in the first area **147**, forming a second device isolation structure **210** in the second area **139, 140** of the semiconductor substrate **150**, forming a first type well **175** with shallow junction in peripheral regions of the second device isolation structure **210** and a region between the first device isolation structure **210, left side in region 139** and the second device isolation structure **210, right side in region 139**, forming a second type well **190** with shallow junction in peripheral region of the first device isolation structure **210** between the first type well with shallow junction **175 (and device isolation 210, right side in area 140),** and defining first and second type active regions on the semiconductor substrate (figures 2a-2i, table 1, and column 11, lines 10-35).

Smayling fails to teach forming the first device isolation region through partial oxidation, forming the second device isolation region with a trench, and forming the second type well with shallow junction in an entire region of the second device isolation structure.

Yoo teaches forming the first device isolation region **7b** through partial oxidation and forming the second device isolation region **9b, 11** with a trench (abstract and column 1, lines 40-43) by teaching that traditional memory cells have been fabricated using thermally grown field oxide regions by a thermal oxidation, and forming a second device isolation **11** with a trench in the second area **2** of the semiconductor substrate (column 1, lines 40-47 and figure 7) by teaching the formation of a trench isolation formation within a MOSFET logic devices and field oxide regions within a memory devices because while field oxides offers acceptable junction leakage needed for memory type devices, trench isolations regions offers greater protection against latch0up phenomena than the LOCOS and field oxide counterparts.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yoo with that of Smayling because traditional memory cells have been fabricated using thermally grown field oxide regions by a thermal oxidation and while field oxides offers acceptable junction leakage needed for memory type devices, trench isolations regions offers greater protection against latch-up phenomena than the LOCOS and field oxide counterparts.

Smayling and Yoo fail to teach forming the second type well with shallow junction in an entire region of the second device isolation structure.

Bohr teaches forming the second type well **38** with shallow junction in an entire region of the second device isolation structure **32b** (figure 6) by teaching the conventional method for formation of forming n well and p well with a channel stop region where the p-well and n-well meet under the device isolation region. The channel stops are used to reduce parasitic current paths, which would result in a loss of current flow.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Bohr with that of Smayling and Yoo because channel stops are used to reduce parasitic current paths, which would result in a loss of current flow.

Regarding claim 5, Bohr teaches the diffusion of ion is simultaneously conducted when the partial oxidation is performed (column 2, lines 7-10 and column 3, line 63 to column 4, lines 18)

Regarding claim 6, Smayling teaches the first type well is an n- type well and the second type well is a p-type well (figure 2i).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smayling et al, US Patent 5,348,895, in view of Yoo et al, US Patent 5,858,830 and Gasner, US Patent 4,599,789.

Regarding claim 7, Smayling teaches a method of forming device isolation structures in an embedded semiconductor device comprising of providing a semiconductor substrate **150** having a first area **147** for a power device in which a first type impurity ions **171** are implanted and a second area **139, 140** for a logic device, forming a first device isolation region **210** in the first area **147**, forming a first type well **171** with deep junction by diffusing the ions in the first area **147**, forming a second device isolation region **210** in the second area **139, 140** of the semiconductor substrate **150**, forming a first type well **175** with shallow junction in peripheral regions of the second device isolation structure **210** and a region between the first device isolation structure and the second device isolation structure with a first photoresist pattern, the first device isolation **210, left side of 139** and the second device isolation, 210, **right side of 139**, forming a second type well **190** with shallow junction in peripheral regions of the first device isolation structure and a region of the second device isolation structure with a second photoresist pattern, and defining first and second type active

regions on the semiconductor substrate (figures 2a-2i, table 1, and column 11, lines 10-35).

Smayling fails to teach forming the first device isolation region through partial oxidation, forming the second device isolation region with a trench, forming a first type well with shallow junction with the first device isolation and the second device isolation having a mask, and forming a second type well with shallow junction with the first device isolation and the second device isolation having a second mask

Yoo teaches forming the first device isolation region **7b** through partial oxidation and forming the second device isolation region **9b, 11** with a trench (abstract and column 1, lines 40-43) by teaching that traditional memory cells have been fabricated using thermally grown field oxide regions by a thermal oxidation, and forming a second device isolation **11** with a trench in the second area **2** of the semiconductor substrate (column 1, lines 40-47 and figure 7) by teaching the formation of a trench isolation formation within a MOSFET logic devices and field oxide regions within a memory devices because while field oxides offers acceptable junction leakage needed for memory type devices, trench isolations regions offers greater protection against latch0up phenomena than the LOCOS and field oxide counterparts.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yoo with that of Smayling because traditional

memory cells have been fabricated using thermally grown field oxide regions by a thermal oxidation and while field oxides offers acceptable junction leakage needed for memory type devices, trench isolations regions offers greater protection against latch-up phenomena than the LOCOS and field oxide counterparts.

Smayling and Yoo fail to teach forming a first type well with shallow junction with the first device isolation and the second device isolation having a mask, and forming a second type well with shallow junction with the first device isolation and the second device isolation having a second mask.

Gasner teaches forming a first type well **46** with shallow junction with the first device isolation **30** and the second device isolation having a mask (figure 9), and forming a second type well **38** with shallow junction with the first device isolation **30** and the second device isolation **30** having a second mask (figures 3) by teaching the conventionally known process and very simple process of forming n-wells and p-wells after formation of the trench isolation regions through the use of a photoresist layer.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gasner with that of Smayling and Yoo because forming n-wells and p-wells after the formation of the device isolation regions using two different photoresist patterns is a simple and conventional process that is commonly used in the art.

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smayling, Yoo, and Gasner as applied to claim 7 above, and further in view of Bohr et al, US Patent 5,091,332 (as cited in previous office actions).

Regarding claim 8, Smayling, Yoo, and Gasner fail to teach the diffusion of ions is simultaneously conducted when the partial oxidation is performed.

Bohr teaches the diffusion of ions is simultaneously conducted when the partial oxidation is performed (column 2, lines 7-10 and column 3, line 63 to column 4, lines 18) by teaching the formation of a field oxide region during the oxidation step, which simultaneously causes the implanted ions to diffuse during the formation of the field oxide. Later, another high temperature step is performed to further diffuse the ions into the substrate. The advantage of these steps is that the second high temperature step causes further diffusion of the ions to form a well without further growing the field oxide step.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Bohr with that of Smayling and Yoo because the advantage of using a wet oxidation process/dry temperature process formation is that that the second high temperature step causes further diffusion of the ions to form a well without further growing the field oxide step.

Regarding claim 9, Smayling teaches the first type well is an n-type well and the second type well is a p-type well (figure 2i).

Response to Arguments

With regards to claim 1, Applicant argues "...Bohr '332 does not, in any way, teach forming a first device isolation region through partial oxidation in the first area and forming a first type well with deep junction by diffusing the ions in the first area *during the same partial oxidation process,* as required by claim 1".

For assertion, Applicant cites "..Bohr '332 goes on to disclose that *after* the implantation step, the substrate is subjected to *a high temperature step,* which comprises a wet high temperature sub-step and a dry high temperature sub-step. In other words, for the wet high temperature step, the substrate is heated in a steam atmosphere to 920°C in order to grow approximately 4600 Angstroms of silicon dioxide as shown in FIG. 4. The field oxide regions 32a, 32b and 32e are grown during this oxidation step. Then, after the wet high temperature step, the substrate is subjected to a dry high temperature step comprising a temperature of 1100°C in a dry nitrogen atmosphere for 4 to 6 hours. *(See,* Bohr '332: col. 3, lines 63 - col. 4, line 7; FIG. 4). After the dry high temperature step, an n-type well 36 is formed beneath the member 26

which extends approximately midway beneath the field oxide region 32b. *(See,* Bohr '332: col. 4, lines 8-11 and FIG. 4)..."

In response to this argument, Bohr states that the high temperature step that is used to grow a field oxide while simultaneously forming an n-type well in the substrate (see column 2, lines 6-9). While Bohr does teach performing a dry high temperature step after performing a wet, high temperature step, Bohr does teach that during the high temperature step at which the field oxides are grown, the previously implanted phosphorus ions also segregate into the substrate as well. The purpose of the dry, high temperature process is to uniformly diffuse in the substrate (see column 4, lines 8-20).

Therefore, the rejection of claims 1-3 under 35 USC 103 (a) is deemed proper.

With regards to claims 4-6, Applicant argues that the prior art fails to teach the limitations of the new claims. In particular, Applicant points out the limitation of "forming a second type well with shallow junction in peripheral regions of the first device isolation structure and *an entire region* of the second device isolation structure between the first type well with shallow junction.

In response to this argument, Examiner points out that due to the claim objection as stated above, there is some confusion as to what this second type well with shallow junction being between which features. Therefore, the cited prior art of record is still

deemed proper for the rejection of these claims, with the Examiner explaining the how the rejection is being maintained.

With regards to claims 7-9, Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 7AM to 3:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QVJ
QVJ

FERNANDO L. TOLEDO
PRIMARY PATENT EXAMINER